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*Effective on 12/8/2004.*
*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*

# FEE TRANSMITTAL
## For FY 2005

| | Complete if Known |
|---|---|
| Application Number | 09/833,953 |
| Filing Date | 04/11/2001 |
| First Named Inventor | Racanelli |
| Examiner Name | Maldonado, Julio J. |
| Art Unit | 2823 |
| Attorney Docket No. | 00CON161P |

☐ Applicant Claims small entity status. See 37 CFR 1.27

| TOTAL AMOUNT OF PAYMENT | $500.00 |
|---|---|

## METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: **50-0731** Deposit Account Name: **Farjami & Farjami LLP**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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## FEE CALCULATION

### 1. BASIC FILING, SEARCH, AND EXAMINATION FEES

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | |

### 2. EXCESS CLAIM FEES

| Fee Description | Small Entity Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent | 50 | 25 |
| Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | | Extra Claims | | Fee ($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|
| | - 20 or HP = | 0 | x | $50.00 | = | $ 0.00 |

HP = highest number of total claims paid for, if greater than 20

| Indep. Claims | | Extra Claims | | Fee ($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|
| | - 3 or HP = | 0 | x | $200.00 | = | $ 0.00 |

HP = highest number of independent claims paid for, if greater than 3

| Multiple Dependent Claims Fee ($) | Fee Paid ($) |
|---|---|
| $360.00 | |

### 3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | | Extra Sheets | | Number of each additional 50 or fraction thereof | | Fee ($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|---|---|
| | - 100 = | 0 | / 50 = | 0 | (round **up** to a whole number) x | $250.00 | = | $ 0.00 |

### 4. OTHER FEE(S)

Non-English Specification, $130 fee (no small entity discount)

Other: **Filing a brief in support of an appeal**

| Fees Paid ($) |
|---|
| **$500.00** |

## SUBMITTED BY

| Signature | | Registration No. (Attorney/Agent) 38135 | Telephone (949) 282-1000 |
|---|---|---|---|
| Name (Print/Type) | Michael Farjami, Esq. | | Date 2/10/06 |

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of: | Art Unit: 2823 |
| **Marco Racanelli** | Examiner: Maldonado, Julio J. |
| Serial No.: 09/833,953 | |
| Filed: April 11, 2001 | |
| For: **Low Cost Fabrication of High Resistivity Resistors** | |

## APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1, 3-12, 14, 15, and 17-23. The Final Rejection issued on October 4, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on December 12, 2005.

## REAL PARTY IN INTEREST

The real party in interest is Newport Fab, LLC dba Jazz Semiconductor.

## RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

## STATUS OF CLAIMS

Claims 1, 3-12, 14, 15, and 17-23 are pending, and claims 2, 13, 16, 24, and 25 were canceled in previous amendments. Claims 1, 3-12, 14, 15, and 17-23 have been finally rejected in a Final Rejection dated October 4, 2005. This Appeal is directed to the rejection of claims 1, 3-12, 14, 15, and 17-23. Claims 1, 3-12, 14, 15, and 17-23 appear in an Appendix to this Appeal Brief.

## STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Rejection dated October 4, 2005.

## SUMMARY OF CLAIMED SUBJECT MATTER

**Claim 1**

Independent claim 1 recites a method including forming (e.g., step 302 of flowchart 300) a layer (e.g., a polycrystalline silicon layer) over a transistor gate region

(e.g., region where gate polycrystalline silicon 226 will be formed) and a field oxide region (e.g., field oxide 208), where the transistor gate region is situated over a well (e.g., N well 218) and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate (e.g., silicon substrate 216). *See*, e.g., page 11, lines 19-22, page 13, lines 15-16, and Figures 2 and 3 of the present application. The method further includes forming (e.g., step 304 of flowchart 300) a doping barrier (e.g., photoresist) above the layer (e.g., the polycrystalline silicon layer) over the field oxide region (e.g., field oxide 208) after the step of forming the layer. *See*, e.g., page 13, lines 18-21 and Figures 2 and 3 of the present application. As disclosed in the present application, the doping barrier can be opened above areas to be N+ implant doped, such as gate polysilicon silicon 226 of structure 200. *See*, e.g., page 14, lines 2-4 and Figure 2 of the present application.

The method further includes doping (e.g., step 306 of flowchart 300) the layer over the transistor gate region (e.g., doping gate polycrystalline silicon 226) with a first dose of a first dopant after the step of forming the doping barrier, where the dose of the first dopant is a dosage greater than required to result in the layer over the transistor gate region having transistor gate electrical properties, and where the first dopant has a first conductivity type. *See*, e.g., page 11, line 22, page 12, lines 1-10, page 14, lines 5-9, and Figures 2 and 3 of the present application. By way of example, gate polycrystalline silicon 226 can be N+ doped using phosphorus dopant with a relatively high dose of approximately $6.5*10^{15}$ atoms per square centimeter, which advantageously allows gate

polycrystalline silicon 226 to be subsequently P type doped along with the resistor comprising polycrystalline silicon layer 202 without affecting the electrical properties of gate polycrystalline silicon 226. *See*, e.g., page 11, line 22 and page 12, lines 1-7 of the present application.

The method further includes removing (e.g., step 308 of flowchart 300) the doping barrier after the step of doping the layer over the transistor gate region with the first dose of the first dopant. *See*, e.g., page 14, lines 10-14 and Figure 3 of the present application. The method further includes doping (e.g., step 308 of flowchart 300) the layer over the transistor gate region and the field oxide region (e.g., doping the entire polycrystalline silicon layer, including polycrystalline silicon layer 202 and gate polycrystalline silicon 226) with a second dose of a second dopant so as to form a high resistivity resistor over the field oxide region (e.g., field oxide 208) after the step of removing the doping barrier, where the second dopant has a second conductivity type, where the first dose of the first dopant is higher than the second dose of the second dopant such that the transistor gate (e.g., gate polycrystalline silicon 226) electrical properties are unaffected by the second dose of the second dopant. *See*, e.g., page 14, lines 10-18 and Figures 2 and 3 of the present application. By way of example, polycrystalline silicon layer 202 and gate polycrystalline silicon 226 can be doped with boron (a P type dopant) at a dose of approximately $1*10^{15}$ atoms per square centimeter. *See*, e.g., page 14, lines 13-16 of the present application.

The method further includes forming (e.g., step 310 of flowchart 300) a silicide blocking oxide layer (e.g., silicon oxide layer 206) over an inner portion of the layer over the field oxide region (e.g., polycrystalline silicon layer 202) after the step of doping the layer over the transistor gate region and the field oxide region with the second dose of the second dopant. *See*, e.g., page 14, lines 20-22, page 15, line 1, and Figures 2 and 3 of the present application. The method further includes doping (e.g., step 310 of flowchart 300) an outer portion of the layer over the field oxide region (e.g., polycrystalline silicon layer 202) with a third dopant so as to form a high-doped region in the outer portion of the layer over the field oxide region after the step of forming the silicide blocking oxide layer over the inner portion of the layer over the field oxide region, where the third dopant has the second conductivity type. *See*, e.g., page 15, lines 1-3 and Figures 2 and 3 of the present application. By way of example, the exposed regions of polycrystalline silicon layer 202 not covered by silicon oxide layer 206 can be P+ doped to enhance electrical connectivity. *See*, e.g., page 15, lines 1-3 and Figure 2 of the present application.

The method further includes fabricating (e.g., step 310 of flowchart 300) a contact region (e.g., silicide contact regions 204) for the high resistivity resistor over the high-doped region in the outer portion of the layer over the field oxide region (e.g., polycrystalline silicon layer 202) after the step of doping an outer portion of the layer over the field oxide region, where the contact region comprises a silicide. *See*, e.g., page 15, lines 3-6 and Figures 2 and 3 of the present application. Thus, as disclosed in the present application, the present invention advantageously forms a high resistivity resistor on the

same chip with other CMOS devices using processing steps which are economical and compatible with CMOS process, where the doping of the resistor is independent of the doping of a PFET gate. *See*, e.g., page 13, lines 2-7 of the present application.

**Claim 14**

Independent claim 14 defines substantially the same subject matter as independent claim 1.

## GROUND(S) OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 3-12, 14, 15, and 17-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,436,177 to Chiara Zaccherini (hereinafter "Zaccherini") in view of U.S. Patent No. 5,489,547 to Erdeljac et al. (hereinafter "Erdeljac") and U.S. Patent No. 6,156,602 to Shao et al. (hereinafter "Shao").

## ARGUMENT

The Examiner has rejected claims 1, 3-12, 14, 15, and 17-23 under 35 U.S.C. §103(a) as being unpatentable over Zaccherini in view of Erdeljac and Shao. For the reasons discussed below, Appellant respectfully submits that the present invention, as defined by independent claims 1 and 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof.

In contrast to the present invention as defined by independent claim 1, Zaccherini does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate.

Zaccherini is directed to a method of manufacturing semiconductor devices by providing a selectively polysilicon pre-amorphousized layer limited to specific areas of the semiconductor device. *See*, e.g., column 2, lines 22-25 of Zaccherini. Zaccherini specifically discloses forming polycrystalline layer 7 over field oxide 5 and channel region 4, where field oxide 5 and channel region 4 are situated in epitaxial layer 3, which is situated over substrate 2. *See*, e.g., column 2, lines 54-55, column 3, lines 1-14, and Figure 3 of Zaccherini. However, Zaccherini fails to teach, disclose, or suggest forming a layer over a transistor gate region, which is situated over a well in a substrate, and

forming the layer over a field oxide region, which is situated in the substrate but not situated over the well, as specified in independent claim 1. In Zaccherini, polycrystalline layer 7 is formed over field oxide 5 and channel region 4, which are situated in epitaxial layer 3. Thus, since Zaccherini requires an additional layer (i.e. epitaxial layer 3) to be formed over substrate 2 prior to forming field oxide 5, channel region 4, and polycrystalline layer 7, the structure disclosed in Zaccherini is substantially different than the structure as specified in independent claim 1. Also, Zaccherini does not teach, suggest, or provide any motivation for forming field oxide 5 and channel region 4 directly in substrate 2 and forming a well in substrate 2.

Additionally, Zaccherini discloses implanting an N type dopant at an implant dosage of between $5x10^{14}$ and $1x10^{16}$ ions/cm$^2$ in polycrystalline layer 7 directly over channel region 4 and subsequently doping polycrystalline layer 7 across the entire wafer with a P type dopant at an implant dosage of between $1x10^{12}$ to $1x10^{15}$ ions/cm$^2$ after removal of photoresist 10, which protected the areas reserved for resistors 8. *See*, e.g., column 3, lines 24-36 and lines 45-53 and Figure 6 of Zaccherini. Thus, in Zaccherini, the respective implant dosage ranges of the N type dopant and the P type dopant overlap. However, independent claim 1 specifies the layer over the transistor gate region is doped with a first dose of a first dopant and, subsequently, the layer over the transistor gate region and the field oxide region is doped with a second dose of a second dopant so as to form a high resistivity resistor over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that the transistor gate

electrical properties are unaffected by the second dose of the second dopant. In contrast, Zaccherini does not require the dosage of the N type dopant to be higher than the dosage of the dosage of the P type dopant that is subsequently implanted in polycrystalline layer 7 across the entire wafer.

Furthermore, Zaccherini fails to teach, disclose, or remotely suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in independent claim 1. In fact, the process disclosed in Zaccherini ends with the step of doping resistors 8 by implantation. Thus, Zaccherini fails to teach, disclose, or suggest the particular sequence of steps as specified in independent claim 1.

In contrast to the present invention as defined by independent claim 1, Erdeljac does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer

over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate.

Erdeljac specifically discloses forming gate 24 in a first polysilicon layer situated over N well 18, which is formed in P- epitaxial layer 12, and forming resistors 32, 34, and 56 in second polysilicon layer 28 on field oxide region 20, which is situated over P- epitaxial layer 12. *See*, e.g., column 1, lines 39-41, column 2, lines 1-19 and 34-36, and Figures 2 and 11 of Erdeljac. Also, in Erdeljac, P- epitaxial layer 12 is formed on P+ substrate 10. *See*, e.g., column 1, lines 31-33 and Figures 1 and 2 of Erdeljac. Thus, in contrast to the present invention as defined by independent claim 1, Erdeljac requires formation of an additional layer (i.e., P- epitaxial layer 12) to be formed on the substrate (i.e., substrate 10) prior to formation of N well 18 and field oxide region 20. Thus, Erdeljac fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in independent claim 1.

Additionally, Erdeljac is teaches formation of polysilicon resistors using a double-level polysilicon process. *See*, e.g., Erdeljac, column 7, lines 9-13. Thus, in Erdeljac, resistors 32, 34, and 56 are formed in second polysilicon layer 28, while gate 24 is formed

in the first polysilicon layer. Thus, Erdeljac fails to teach, disclose, or remotely suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in independent claim 1. Thus, by using a double-level polysilicon process so as to form polysilicon resistors in one polysilicon layer and a gate in another polysilicon layer, Erdeljac discloses a method and resulting structure that is substantially different than the method and resulting structure specified in independent claim 1.

Furthermore, in Erdeljac, a metal layer is deposited, patterned, and etched to form contacts 54 for contacting end portions 32b and 32c of resistor 32 and end portions of resistors 34 and 56. *See*, e.g., column 6, lines 16-21 and Figure 11 of Erdeljac. However, Erdeljac fails to teach, disclose, or remotely suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and, next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as

specified in independent claim 1. Thus, Erdeljac fails to cure the basic deficiencies of Zaccherini discussed above.

On pages 3 and 4 of the Final Rejection dated October 4, 2005, the Examiner states:

> "[i]t would have been within the scope of one of ordinary skill in the art to combine the teachings of Zaccherini and Erdeljac et al. to enable forming the gate transistors and field oxide regions of Zaccherini on the substrate of Erdeljac et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative methods of forming gate electrodes and field oxide regions of Zaccherini and art recognized suitability for an intended purpose has been recognized to be motivation to combine."

However, the fabrication method and resulting structure disclosed in Erdeljac is substantially different than the fabrication method and resulting structure disclosed in Zaccherini. For example, Zaccherini discloses forming a P doped resistor and a gate terminal in the same polycrystalline layer (i.e., polycrystalline layer 7). In contrast, as discussed above, Erdeljac discloses a double-level polysilicon process that results in the formation of a gate (i.e., gate 24) in a first polysilicon layer and formation of resistor (i.e., resistors 32, 34, and 56) in a second polysilicon layer (i.e., second polysilicon layer 28). In **In re Gordon**, 733 F.2d 900, 902 (Fed. Cir. 1984), the Federal Circuit has set forth the obviousness determination (see also **In re Fitch**, 972 F.2d 1260 (Fed. Cir. 1992)):

> "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious *unless the prior art suggested the desirability of the modification*" (emphasis added).

Thus, for the above reasons, Appellant respectfully submits that the combination of Zaccherini and Erdeljac suggested by the Examiner is not based on any evidence of reason in the prior art that would have suggested to one of ordinary skill in the art the desirability of such modifications. Rather, the reason, suggestion and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Appellant's disclosure.

In contrast to the present invention as defined by independent claim 1, Shao does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate.

Shao specifically discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate (e.g., NMOS gate 40) while masking the PMOS region of poly 2 layer 16. *See*, e.g., column 5, lines 11-17 and Figure 1 of Shao. In Shao, the doping (i.e., N+ implant 18) for the N+ poly gate structure is also applied to the region in poly 2 layer 16 (i.e., the region in poly 2 layer 16 situated over field oxide regions 12) where the load resistor (e.g., load resistor 38) is to be formed so as to control the value that is established for the load resistor. *See*, e.g., column 5, lines 22-26 and Figures 1 and 5 of Shao. Thus, Shao fails to teach, disclose, or remotely suggest sequentially forming a doping barrier above a layer over a field oxide region, doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, removing the doping barrier, and doping the layer over the transistor gate region and the field oxide region with a second dose of a second dopant having a second conductivity type, as specified in independent claim 1.

Additionally, in Shao, NMOS gate 40, PMOS gate 46, load resistor 38, and field oxide regions 12 are all formed on substrate 10. *See*, e.g., column 7, lines 15-23 and Figure 5 of Shao. However, Shao fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where the field oxide region and the well are situated in a substrate, as specified in independent claim 1. Moreover, Shao fails to teach, disclose, or suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then

doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and, next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in independent claim 1.

As discussed above, independent claim 1 recites a series of steps that are performed in a specified sequence to advantageously achieve a low cost high resistivity resistor. However, the particular sequence of step specified in independent claims is not disclosed, taught, or suggested in Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof. Thus, Appellant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggested by the Examiner does not and cannot result in the invention as defined by independent claim 1.

On page 5 of the Final Rejection dated October 4, 2005, the Examiner states:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac et al. with the teachings of Shao et al. to enable forming high doping areas and electrical contacts in the high resistivity resistor of Zaccherini and Erdeljac et al., as taught by Shao et al., since this would result in the formation of electrical points of contact (column 8, lines 9-10)."

However, as discussed above, the fabrication method and resulting structure disclosed in Erdeljac is substantially different than the fabrication method and resulting structure disclosed in Zaccherini. Additionally, the fabrication method and resulting structure disclosed in Shao is substantially different than the fabrication method and

resulting structure disclosed in either Erdeljac or Zaccherini. For the above reasons, Appellant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggested by the Examiner is not based on any evidence of reason, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to make such modifications. Rather, the reason, suggestion and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Appellant's disclosure.

For the foregoing reasons, Appellant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 3-12 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Independent claim 14 recites similar limitations as independent claim 1 discussed above. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 14, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao. As such, the present invention, as defined by independent claim 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 15 and 17-23 depending from independent claim 14 are, *a fortiori*, also

patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

## CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 14 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-12, 14, 15, and 17-23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 3-12, 14, 15, and 17-23 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Michael Farjami, Esq.
Reg. No. 38, 135

Date: 2/10/06

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Date of Deposit: 2/10/06

Christina Carter
Name of Person Mailing Paper and/or Fee

Christina Carter 2/10/06
Signature Date

# APPENDIX OF CLAIMS ON APPEAL

**Claim 1:** A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region, said transistor gate region being situated over a well and said field oxide region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said layer over said field oxide region after said step of forming said layer;

doping said layer over said transistor gate region with a first dose of a first dopant after said step of forming said doping barrier, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier after said step of doping said layer over said transistor gate region with said first dose of said first dopant;

doping said layer over said transistor gate region and said field oxide region with a second dose of a second dopant so as to form a high resistivity resistor in said layer over said field oxide region after said step of removing said doping barrier, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region after said step of doping said layer over said transistor gate region and said field oxide region with said second dose of said second dopant;

doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region after said step of forming said silicide blocking oxide layer over said inner portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type;

fabricating a contact region for said high resistivity resistor over said high-doped region in said outer portion of said layer over said field oxide region after said step of doping an outer portion of said layer over said field oxide region, wherein said contact region comprises a silicide.

**Claim 3:** The method of claim 1 wherein said layer comprises polycrystalline silicon.

**Claim 4:** The method of claim 1 wherein said transistor gate region is a gate of an PFET.

**Claim 5:** The method of claim 1 wherein said transistor gate region is a gate of an NFET.

**Claim 6:** The method of claim 1 wherein said field oxide comprises silicon dioxide.

**Claim 7:** The method of claim 1 wherein said first dopant is an N type dopant.

**Claim 8:** The method of claim 7 wherein said N type dopant comprises phosphorous.

**Claim 9:** The method of claim 1 wherein said first dopant comprises phosphorous at a dose of approximately $6.5x10^{15}$ atoms per square centimeter.

**Claim 10:** The method of claim 1 wherein said second dopant is a P type dopant.

**Claim 11:** The method of claim 10 wherein said P type dopant comprises boron.

**Claim 12:** The method of claim 1 wherein said second dopant comprises boron at a dose of approximately $1.0x10^{15}$ atoms per square centimeter.

**Claim 14:** A method comprising steps of:

depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon

layer including a gate region and a resistor region, said gate region being situated over a well and said resistor region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said polycrystalline silicon layer after said step of depositing said polycrystalline silicon layer so as to prevent doping of said resistor region of said polycrystalline silicon layer;

doping said polycrystalline silicon layer with a first dose of a first dopant after said step of forming said doping barrier, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier after said step of doping said polycrystalline silicon layer with said first dose of said first dopant;

doping said polycrystalline silicon layer with a second dose of a second dopant after said step of removing said doping barrier so as to form a high resistivity resistor in said resistor region of said polycrystalline silicon, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said polycrystalline silicon layer over said field oxide region after said step of doping said polycrystalline silicon layer with said second dose of said second dopant;

doping an outer portion of said resistor region of said polycrystalline silicon layer with a third dopant after said step of forming said silicide blocking oxide layer so as to form a high-doped region in said outer portion of said resistor region, wherein said third dopant has said second conductivity type;

fabricating a contact region over said high-doped region in said outer portion of said resistor region of said polycrystalline silicon layer after said step of doping said outer portion of said resistor region of said polycrystalline silicon layer, said contact region being electrically connected to said resistor region, wherein said contact region comprises a silicide.

**Claim 15:** The method of claim 14 wherein said doping barrier comprises photoresist.

**Claim 17:** The method of claim 14 wherein said step of doping said polycrystalline silicon layer with a first dopant comprises doping said gate region.

**Claim 18:** The method of claim 14 wherein said first dopant is an N type dopant.

**Claim 19:** The method of claim 18 wherein said N type dopant comprises phosphorous.

**Claim 20:** The method of claim 14 wherein said first dopant comprises phosphorous at a dose of approximately $6.5x10^{15}$ atoms per square centimeter.

**Claim 21:** The method of claim 14 wherein said second dopant is a P type dopant.

**Claim 22:** The method of claim 21 wherein said P type dopant comprises boron.

**Claim 23:** The method of claim 14 wherein said second dopant comprises boron at a dose of approximately $1.0x10^{15}$ atoms per square centimeter.

# EVIDENCE APPENDIX

**(NONE)**

# RELATED PROCEEDINGS APPENDIX

**(NONE)**